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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte DAVID R. HEMBREE and ALAN G. WOOD

Appeal 2009-005567
Application 09/933,492[1]
Technology Center 2800

Decided: November 19, 2009

Before SCOTT R. BOALICK, JOHN A. JEFFERY, and
MARC S. HOFF, *Administrative Patent Judges*.

BOALICK, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] Application filed August 20, 2001. The real party in interest is Micron Technology, Inc.

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 52-62 and 70-77, all the claims pending in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

STATEMENT OF THE CASE

Appellants' invention relates to a method for fabricating and testing semiconductor components that uses testing data to etch a pattern of redistribution conductors that can be configured to, among other things, repair, reconfigure, or electrically isolate selected semiconductor components. (Spec. 2:2-4, 4:10 to 5:30.)

Claim 52 is exemplary:

52. A semiconductor component comprising:

> a substrate comprising a plurality of semiconductor components, each component including a plurality of component contacts and a plurality of integrated circuits in electrical communication with the component contacts, the components including a plurality of good components and at least one defective component; and
>
> a plurality of redistribution conductors on the components in electrical communication with the component contacts configured to repair the defective component, the conductors having a pattern containing information from testing of the semiconductor components representing locations of the good components, the defective component and the component contacts, and for repairing the defective component.

The prior art relied upon by the Examiner in rejecting the claims on appeal is:

Tanizawa	4,721,995	Jan. 26, 1988

Claims 52-62 and 70-77 stand rejected under 35 U.S.C. § 112, second paragraph, as being indefinite.

Claims 52-62 and 70-77 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Tanizawa.

Only those arguments actually made by Appellants have been considered in this decision. Arguments that Appellants did not make in the Brief[2] have not been considered and are deemed to be waived. *See* 37 C.F.R. § 41.37(c)(1)(vii).

ISSUES

Initially, we note that Appellants present arguments (Reply Br. 11-13) regarding drawing and new matter objections made by the Examiner in the Final Office Action and the Answer, but which were not maintained in the Supplemental Answer. These objections are not appealable matters for the Board and we will not consider them further. *See* MPEP § 1201 ("The line of demarcation between appealable matters for the Board of Patent Appeals and Interferences (Board) and petitionable matters for the Director of the U.S. Patent and Trademark Office (Director) should be carefully observed. The Board will not ordinarily hear a question that should be decided by the Director on petition.").

We also note that the Examiner's Supplemental Answer has withdrawn the rejection of claims 52, 56, 60, and 70 under 35 U.S.C. § 112, first paragraph, due to insufficient written description. (Supp. Ans. 12.)

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[2] The Reply Brief filed December 24, 2008 states that it "replaces the Amended Appeal Brief filed by Appellant on 03/22/2007, and the Rebuttal Brief filed by Appellant on 08/16/2007." (Reply Br. 1.)

§ 112, Second Paragraph Rejection

Appellants argue that the Examiner erred in rejecting the claims as indefinite. (Reply Br. 14-15.) In particular, Appellants argue that one of ordinary skill in the art would understand what is being claimed when the claim limitations "a plurality of redistribution conductors . . . in electrical communication with the component contacts *configured to repair the defective component*" (emphasis added) and "the conductors *having a pattern containing information from testing* of the semiconductor components . . . for repairing the defective component" (emphasis added) are read in light of the Specification. (Reply Br. 14-15.)

Appellants' arguments present the following issue:

Have Appellants shown that the Examiner erred in rejecting claims 52-62 and 70-77 under 35 U.S.C. § 112, second paragraph?

The resolution of this issue turns on the following subsidiary issues:

1. Have Appellants shown that the Examiner erred in finding that one of ordinary skill in the art would not understand what is being claimed when the limitation "a plurality of redistribution conductors . . . in electrical communication with the component contacts configured to repair the defective component" is read in light of the Specification?

2. Have Appellants shown that the Examiner erred in finding that one of ordinary skill in the art would not understand what is being claimed when the limitation "the conductors having a pattern containing information from testing of the semiconductor components . . . for repairing the defective component" is read in light of the Specification?

§ 102(b) Rejection

Appellants argue that the Examiner erred in finding that Tanizawa anticipates the claims. (Reply Br. 16-21.) In particular, Appellants argue that Tanizawa does not teach "redistribution conductors" as claimed because the circuit patterns 6 of Tanizawa are on different components and interconnect circuit blocks 2 (Reply Br. 16), that they "cannot and do not perform the function of redistribution conductors" (Reply Br. 16; *see also* Reply Br. 21), that they do not contain information from the testing of the semiconductor components (Reply Br. 17), and that they are wiring patterns on a separate film which interconnect components rather than being an integrated structure (Reply Br. 17, 21). In addition, Appellants argue that the circuit patterns 6 of Tanizawa are not configured to repair a defective component as recited by independent claims 52 and 70 (Reply Br. 18, 19, 21), electrically isolate a defective component as recited by independent claims 56 and 70 (Reply Br. 18, 19, 21), reconfigure a defective component as recited by independent claims 60 and 70 (Reply Br. 18, 20, 21), or connect good components in clusters as recited by independent claim 70 (Reply Br. 18, 21). With respect to claim 70, Appellants also argue that Tanizawa does not teach a metal redistribution layer, as claimed. (Reply Br. 21.)

Appellants' arguments present the following issue:

Have Appellants shown that the Examiner erred in rejecting claims 52-62 and 70-77 under 35 U.S.C. § 102(b)?

The resolution of this issue turns on the following subsidiary issues:

1. Have Appellants shown that the Examiner erred in finding that Tanizawa teaches "redistribution conductors," as claimed?

2. Have Appellants shown that the Examiner erred in finding that Tanizawa teaches a "metal redistribution layer"?

FINDINGS OF FACT

The record supports the following findings of fact (FF) by a preponderance of the evidence.

Appellants' Specification

1. Appellants describe testing a semiconductor substrate 10 that contains a plurality of semiconductor components 12 in order to identify good components 12 and defective components 12D. (Spec. 7:8-30; Figs. 2A, 2B, 4.) A metal redistribution layer 20 is then deposited on the substrate and patterned to form patterns of conductors 22 on the components 12. (Spec. 10:13-30; Figs. 2C, 2F.)

2. In one embodiment, a radiant sensitive film 24 is formed on the redistribution layer 20. (Spec. 10:31-32; Fig 2D.) A laser scanner 26 receives digital data 36 representing a selected pattern to be written on the radiant sensitive film 24. (Spec. 11:17-20; 12:1-5; Fig. 3.) The digital data 36 includes test data such as, for example, the location of defective components 12D. (Spec. 12:8-15.) The laser scanner 26 is used to expose and develop the radiant sensitive film 24 to form a mask 25 which will then be used to etch the redistribution layer 20 into a pattern of conductors 22. (Spec. 12:27-33; Figs. 2E, 2F.)

3. Appellants' Specification states that:

> [T]he redistribution layer 20 can be etched with the conductors 22 in patterns selected to achieve different objectives. As a first example, the redistribution layer 20 can be etched to repair or re-configure defective components 12D (Figures 4 and 5). Specifically, the initial testing step identifies the defective components 12D and this information is contained in the digital data 36 (Figure 3) supplied to the modulator 34. Some defects can be corrected by providing conductors 22 that substitute redundant circuitry contained on the defective components 12D for defective circuitry.
>
> Other defects can be corrected by configuring or re configuring the component 12D in a particular electrical format. For example, a memory component (e.g., DRAM) may be defective when configured as a 1 Meg X 16 device (i.e., 1 megabit deep by 16 bits wide = 16 megabits of total memory). However, the memory component may not be defective when configured as a 4 Meg X 4 device (i.e., 4 megabits deep by 4 bits wide = 16 megabits of total memory). By electrically connecting, or alternately electrically isolating, selected component contacts 28 using the conductors 22 different configurations can be achieved.
>
> As also shown in Figure 1, and illustrated in Figure 4, the redistribution layer 20 can be etched with patterns of conductors 22 that electrically isolate the defective components 12D.

(Spec. 13:22 to 14:13.)

Tanizawa

4. Tanizawa describes a very large scale integrated (VLSI) circuit semiconductor device formed on a wafer. (Abstract; col. 1, ll. 6-15.) A number of isolated circuit blocks are formed in a matrix on the wafer and are connected to interconnecting circuits to complete the

wafer integrated circuit. (Abstract.) The interconnecting circuits are formed on an insulative film and placed on the wafer. (Abstract; col. 2, ll. 30-34, 50-52.) The circuit blocks are tested in advance by computer aided testing apparatus and defective circuit blocks are replaced by repair chips without requiring rework of the interconnecting circuits. (Abstract.) Repair chips are aligned with and bonded on the bad circuit blocks. (Col. 2, l. 67 to col. 3, l. 9.) Two methods of wiring the repair chip are disclosed. (Col. 3, l. 14 to col. 4, l. 17.) One method places the flexible insulative film on the mended wafer where the bonding pads on the wafer are aligned with and bonded to the wiring pattern on the flexible insulative film. (Col. 3, ll. 59-68.)

5. In one embodiment, a number of circuit blocks 2, each having pads 4 in a predetermined layout pattern, are formed on a silicon wafer 1. (Col. 5, ll. 1-27; Figs. 3(a), 3(b).) An interconnecting film to be placed on the wafer 1 includes an insulative film 5 and an interconnecting circuit pattern 6 that may be formed on the top surface and the rear surface of the film 5 and interconnected through holes in the film 5. (Col. 5, ll. 28-41; Fig. 3(b).) The circuit patterns 6 may be made of copper and have bonding pads 6B on the rear surface of the film 5 that correspond to the bonding pads 4 of the circuit blocks 2 of the wafer 1. (Col. 5, ll. 36-39, 42-50.) The interconnecting film is aligned on the wafer 1 and each corresponding pad 4 and pad 6B is bonded. (Col. 5, ll. 51-56; Fig. 3(b).)

6. Tanizawa teaches that bad portions or bad circuit blocks are detected by a testing process and are replaced with repair chips 8. (Col. 5, ll. 58-66; Figs. 4, 6(a), 6(b).) The replacement of the bad circuit blocks is performed without rework of the interconnecting circuit. (Col. 5, l. 67 to col. 6, l. 3.) In one embodiment, a repair chip 8 is bonded to the pads 4 of a bad circuit block 2. (Col. 6, ll. 13-14, 21-23.) A flexible insulative film 10 is deformed to cover the protruding repair chip 8 and the pads 9 of the repair chip 8 and bonding means 11B of the interconnecting circuit are electrically connected. (Col. 6, ll. 10-14, 25-30; Fig. 6(b).) "Thus the circuit blocks 2 including the repair chip 8 are connected to the interconnecting circuit pattern 6." (Col. 6, ll. 31-32; Fig. 6(b).)

PRINCIPLES OF LAW

The purpose of the second paragraph of 35 U.S.C. § 112 "is to provide those who would endeavor, in future enterprise, to approach the area circumscribed by the claims of a patent, with the adequate notice demanded by due process of law, so that they may more readily and accurately determine the boundaries of protection involved and evaluate the possibility of infringement and dominance." *In re Hammack*, 427 F.2d 1378, 1382 (CCPA 1970). The test for definiteness under the second paragraph of 35 U.S.C. § 112 is "whether those skilled in the art would understand what is claimed when the claim is read in light of the specification." *Orthokinetics, Inc. v. Safety Travel Chairs, Inc.*, 806 F.2d 1565, 1576 (Fed. Cir. 1986).

Anticipation is established when a single prior art reference discloses, expressly or under the principles of inherency, each and every limitation of

the claimed invention. *Atlas Powder Co. v. IRECO, Inc.*, 190 F.3d 1342, 1347 (Fed. Cir. 1999); *In re Paulsen*, 30 F.3d 1475, 1478-79 (Fed. Cir. 1994).

During examination of a patent application, a claim is given its broadest reasonable construction consistent with the specification. *In re Prater*, 415 F.2d 1393, 1404-05 (CCPA 1969). "[T]he words of a claim 'are generally given their ordinary and customary meaning.'" *Phillips v. AWH Corp.*, 415 F.3d 1303, 1312 (Fed. Cir. 2005) (en banc) (internal citations omitted). The "ordinary and customary meaning of a claim term is the meaning that the term would have to a person of ordinary skill in the art in question at the time of the invention, i.e., as of the effective filing date of the patent application." *Id.* at 1313.

ANALYSIS

Appellants' arguments that the Examiner erred in rejecting claims 52-62 and 70-77 as being indefinite are persuasive. However, Appellants have not shown that the Examiner erred in rejecting claims 52-62 and 70-77 as being anticipated by Tanizawa.

§ 112, Second Paragraph Rejection

Appellants' arguments that the Examiner erred in rejecting claims 52-62 and 70-77 as being indefinite are persuasive. We agree with Appellants that, when read in light of the Specification, one of ordinary skill in the art would understand what is being claimed by "a plurality of redistribution conductors . . . in electrical communication with the component contacts configured to repair the defective component" and "the

conductors having a pattern containing information from testing of the semiconductor components . . . for repairing the defective component."

Regarding the limitation "a plurality of redistribution conductors . . . in electrical communication with the component contacts *configured to repair the defective component*" (emphasis added), Appellants' Specification explains that a redistribution layer 20 can be used to repair defective components 12D. (FF 3.) The Specification further explains that "[s]ome defects can be corrected by providing conductors 22 that substitute redundant circuitry contained on the defective components 12D for defective circuitry." (FF 3.) Thus, the Specification teaches that defective components can be repaired by using the redistribution conductors to substitute good redundant circuitry for the defective circuitry.

Regarding the limitation "the conductors *having a pattern containing information from testing* of the semiconductor components . . . for repairing the defective component" (emphasis added), the Specification teaches that an initial testing step identifies defective components and this information is used to etch the redistribution layer 20 into a pattern of conductors 22 to repair the defect in the manner previously discussed. (FF 1-3.) Thus, by connecting only good components, the pattern of conductors contains the information from the initial testing step.

Accordingly, we conclude that Appellants have shown that the Examiner erred in rejecting claims 52-62 and 70-77 under 35 U.S.C. § 112, second paragraph.

§ 102(b) Rejection

Appellants' arguments that the Examiner erred in rejecting claims 52-62 and 70-77 as being anticipated by Tanizawa are not persuasive. Instead, we agree with the Examiner (Ans. 5-6, 14-21) that Tanizawa teaches "redistribution conductors," as claimed.

The claims broadly recite a "redistribution conductor." While the Specification teaches that a metal redistribution layer 20 may be blanket deposited on a substrate 10 and etched to form a pattern of conductors 22 and that redistribution layers are well known (Spec. 10:13-30; *see also* FF 1-3), the Specification does not prohibit other conductors from being redistribution conductors. We decline Appellants' invitation (Reply Br. 16) to import these limitations from the Specification into the claims.

Under the broadest reasonable interpretation consistent with the Specification, we agree with the Examiner (Ans. 5-6, 14-21) that Tanizawa teaches redistribution conductors by teaching an interconnecting film with interconnecting circuit patterns 6 having bonding pads 6B. (FF 4-6.) Appellants have not provided any convincing evidence or argument that the claims require an integrated structure or exclude wiring patterns on a separate film that interconnect circuit blocks. By connecting only to good components, including repair chips 8, the interconnecting circuit patterns 6 are configured to repair a defective component, electrically isolate the contacts of a defective component, or reconfigure the contacts of a defective component in a manner consistent with the Specification. (FF 4-6; *see also* FF 3.) In addition, by testing the circuit blocks 2 and only connecting to good circuit components, including repair chips 8, Tanizawa teaches that the

circuit patterns 6 contain information from the testing of the components in a manner consistent with the Specification. (FF 4-6; *see also* FF 3.)

Thus, we find unconvincing Appellants' arguments that the circuit patterns 6 of Tanizawa are on different components and interconnect circuit blocks 2 (Reply Br. 16), that they "cannot and do not perform the function of redistribution conductors" (Reply Br. 16; *see also* Reply Br. 21), that they do not contain information from testing of the semiconductor components (Reply Br. 17), and that they are wiring patterns on a separate film which interconnect components rather than being an integrated structure (Reply Br. 17, 21).

Claims 52-55

Appellants also argue that the circuit patterns 6 of Tanizawa are not configured to repair a defective component, as recited by independent claim 52 (Reply Br. 18, 19). We do not agree.

The Specification teaches that a defective component may be repaired by substituting redundant circuitry in place of the defective circuitry. (FF 3.) In addition, as the Examiner points out (Ans. 18), the claims do not limit the manner in which the repair function is performed. Tanizawa teaches that a repair chip 8 is used to replace a defective circuit, and that the interconnecting circuit 6 is then connected to the repair chip 8 rather than to the defective circuit. (FF 4-6.) Thus, consistent with the Specification, the circuit patterns 6 of Tanizawa are configured to repair a defective component.

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting independent claim 52 under 35 U.S.C. § 102(b). Claims 53-55 were not argued separately, and fall together with claim 52.

Claims 56-59

Appellants further argue that the circuit patterns 6 of Tanizawa are not configured to electrically isolate a defective component, as recited by independent claim 56 (Reply Br. 18, 19). We do not agree.

While Appellants admit that "the circuit patterns 6 in Tanizawa are configured to electrically isolate defective circuit blocks 2" (Reply Br. 19), Appellants repeat the argument that the circuit patterns 6 of Tanizawa are not redistribution conductors but, rather, are traces on an insulative film located between circuit blocks 2 (Reply Br. 19). We do not agree with this argument for the reasons previously discussed. The isolation performed by Tanizawa, as admitted by Appellants, fully meets that claimed by claim 56.

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting independent claim 56 under 35 U.S.C. § 102(b). Claims 57-59 were not argued separately, and fall together with claim 56.

Claims 60-62

Appellants also argue that the circuit patterns 6 of Tanizawa are not configured to reconfigure a defective component, as recited by independent claim 60 (Reply Br. 18, 20). Appellants contend that the Specification "states what is meant by the term 'reconfigure'" (Reply Br. 20; *see also* FF 3) and that the circuit patterns 6 do not perform a reconfiguration because the

repair chip 8 of Tanizawa replaces the defective circuit block 2. (Reply Br. 20.) We do not agree.

Although the Specification gives a non-limiting example of a reconfiguration of a component (FF 3), it does not prohibit other methods of performing a reconfiguration function. As the Examiner correctly points out (Ans. 19), the claims do not specify how the defective component is to be reconfigured. Accordingly, we agree with the Examiner (Ans. 19, 20) that the reconfiguration disclosed by Tanizawa meets the claimed reconfiguration function.

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting independent claim 60 under 35 U.S.C. § 102(b). Claims 61 and 62 were not argued separately, and fall together with claim 60.

Claims 70-77

Appellants further argue that the circuit patterns 6 of Tanizawa are not configured to repair, reconfigure, or electrically isolate a defective component, or to connect good components in clusters, as recited by independent claim 70. (Reply Br. 18, 21.) Appellants also argue that Tanizawa does not teach a metal redistribution layer, as recited by independent claim 70. (Reply Br. 21.) We do not agree.

As previously discussed, the circuit patterns 6 of Tanizawa are configured to repair a defective component, electrically isolate a defective component, and reconfigure a defective component. In addition, we agree with the Examiner (Ans. 10, 11, 20, 21) that Tanizawa teaches a metal redistribution layer by teaching circuit patterns 6 made of copper on a

substrate 1. (FF 5.) Alternatively, Tanizawa teaches a metal redistribution layer by teaching circuit patterns 6 made of copper on a substrate 5. (FF 5.)

Accordingly, we conclude that Appellants have not shown that the Examiner erred in rejecting independent claim 70 under 35 U.S.C. § 102(b). Claims 71-77 were not argued separately, and fall together with claim 70.

CONCLUSION

Based on the findings of fact and analysis above, we conclude that:

(1) Appellants have shown that the Examiner erred in rejecting claims 52-62 and 70-77 under 35 U.S.C. § 112, second paragraph.

(2) Appellants have not shown that the Examiner erred in rejecting claims 52-62 and 70-77 under 35 U.S.C. § 102(b).

DECISION

The rejection of claims 52-62 and 70-77 under 35 U.S.C. § 112, second paragraph is reversed.

The rejection of claims 52-62 and 70-77 under 35 U.S.C. § 102(b) is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED

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